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CMOS-Compatible Catalyst for MacEtch: Titanium Nitride-Assisted Chemical Etching in Vapor phase for High Aspect Ratio Silicon Nanostructures

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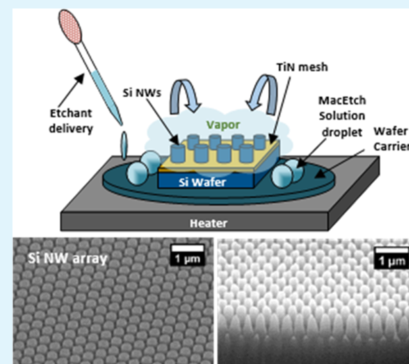
Supporting Information

ABSTRACT: Metal-assisted chemical etching (MacEtch) is an emerging anisotropic chemical etching technique that has been used to fabricate high aspect ratio semiconductor micro- and nanostructures. Despite its advantages in unparalleled anisotropy, simplicity, versatility, and damage-free nature, the adaptation of MacEtch for silicon (Si)-based electronic device fabrication process is hindered by the use of a gold (Au)-based metal catalyst, as Au is a detrimental deep-level impurity in Si. In this report, for the first time, we demonstrate CMOS-compatible titanium nitride (TiN)-based MacEtch of Si by establishing a true vapor-phase (VP) MacEtch approach in order to overcome TiN-MacEtch-specific challenges. Whereas inverse-MacEtch is observed using conventional liquid phase MacEtch because of the limited mass transport from the strong adhesion between TiN and Si, the true VP etch leads to forward MacEtch and produces Si nanowire arrays by engraving the TiN mesh pattern in Si. The etch rate as a function of etch temperature, solution concentration, TiN dimension, and thickness is systematically characterized to uncover the underlying nature of MacEtching using this new catalyst. VP MacEtch represents a significant step toward scalability of this disruptive technology because of the high controllability of gas phase reaction dynamics. TiN-MacEtch may also have direct implications in embedded TiN-based plasmonic semiconductor structures for photonic applications.



KEYWORDS: *Titanium nitride, CMOS-compatible, metal-assisted chemical etching, vapor-phase MacEtch, silicon, nanowire*

INTRODUCTION

Metal-assisted chemical etching (MacEtch) is a local electrochemical etching method capable of producing anisotropic high aspect ratio semiconductor structures with a simple wet etching process catalyzed by a patterned metal film.[1−3] MacEtch eliminates high-energy ion-induced damage and sidewall scallops that typically occur in conventional deep reactive ion etching.[4] Nanowires (NW), vias, trenches, and other surface textures have been demonstrated using MacEtch for silicon (Si), germanium (Ge), and compound semiconductors (GaAs, InGaAs, InP, GaP, GaN, β-Ga_2O_3), either in the forward or inverse manner relative to the catalyst location.[5−10] They have been used as the building blocks in electronic and optoelectronic device applications such as light-emitting diodes, solar cells, photodetectors, biosensors, super capacitors, thermo-electrics, and FinFETs.[8,9,11−16]

Typical Si MacEtch starts by depositing a noble metal catalyst film such as gold (Au), platinum (Pt), or silver (Ag) on the semiconductor surface. The catalyst can be patterned into any arbitrary geometry by a variety of lithography or non-lithographical methods. Then, the sample is immersed in a solution mixture of n acid (e.g., hydrofluoric acid (HF)) and an oxidant (e.g., hydrogen peroxide (H_2O_2)) to selectively oxidize and dissolve the semiconductor localized under the catalyst.[1−3] During MacEtch, at the liquid−catalyst interface, electronic holes are produced by the reduction reaction of the oxidant (cathodic reaction), which are injected in the valence band to produce oxidized semiconductor (anodic reaction) that is subsequently dissolved by the acid.[1] The process of electronic holes generated and injected into the semiconductor is defined as the carrier generation step and the transport of the etchant and byproducts is defined as the mass transport step.[17] The etch rate is affected by both the carrier generation and mass transport steps: in the carrier generation-dominant

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regime, the etch rate is governed by the amount of the holes injected in the semiconductor, and in the mass transport dominant regime, it is governed by how fast the oxidized semiconductor can be removed so that the next pristine semiconductor surface is exposed for the next oxidation cycle to start. Because of the material dissolution taking place laterally underneath the catalyst surface, the mass transport rate is influenced by the size of catalyst and the van der Waals force between the catalyst and semiconductor.[18−20] On the other hand, carrier generation is affected by the electrochemical potential of the oxidant and the metal catalyst,[16] and the metal−semiconductor barrier height that is defined by the band gap, electron affinity, and doping concentration of the semiconductor and metal work function.[10,21] Noble metals of Au, Ag, Pt, Pd, Cu have been reported as MacEtch catalysts[3] and showed that the etch rate and porosity can be engineered by using metals with different electrochemical potentials.

Despite its simplicity of producing high aspect ratio complex semiconductor structures, using noble metal catalyst, especially Au, is the major limitation for MacEtch to be applied in electronic device applications specifically in the front end of the line (FEOL) and back end of the line (BEOL) in the complementary metal-oxide semiconductor (CMOS) fabrication process because of the deep-level defects concern.[22] In order for MacEtch to be applied in the CMOS process, the catalyst not only has to be CMOS-compatible but also has to satisfy the MacEtch catalyst requirements of hole generation and injection capability, as well as high HF chemical resistivity. Recently, nonconventional metal material with high conductivity has been investigated as the MacEtch catalyst. Graphene-assisted chemical etching (GaCE) was demonstrated by Kim et al. in 2013.[23] The authors patterned the transferred graphene on a Si substrate using anodic aluminum oxides as the patterning templates, then, etched the sample in HF and H_2O_2 at temperatures of 40−50 °C to form nanopillar arrays with a aspect ratio as high as ∼6:1. However, GaCE is sensitive to the structural nonuniformity of graphene resulted from the grain boundaries and point defects such that the uniformity of the nanopillar array across the graphene mesh formed by GaCE was poor. In addition, any Cu residue from the wet or dry transfer can lead to the formation of deep-level defects. Therefore, the GaCE using transferred graphene is still not CMOS-compatible at this stage.

In this work, for the first time, we present a fully CMOS-compatible MacEtch demonstration using titanium nitride (TiN) as the catalyst. TiN is a particularly attractive material because of its CMOS compatibility. TiN has been used as a diffusion barrier or electromigration blocking layer for metal interconnects in modern integrated circuits, because of its low resistivity, high thermal stability, mechanical durability, and excellent step coverage.[24] TiN is chemically resistive to HF,[25,26] has a electrochemical potential between 0.5 and 0.9 V,[27] and a work function of 4.5 eV;[28] thus, it is suitable to serve as a MacEtch catalyst. However, the adhesion and Young's modulus of TiN on Si is known to be much stronger than Au on Si,[29] resulting in distinctly different etching behavior compared to Au-MacEtch. van der Waals force is one of the dominant sources of attraction between Si and the catalyst.[18,19] After each cycle of carrier generation and mass transport reactions, the catalyst adheres to the semiconductor surface by the van der Waals force.[18] In the case of TiN−Si, because of the strong adhesion at the interface, it is difficult for the mass transport reaction to take place laterally underneath the catalyst. In addition, the catalyst cannot be easily conformal to the etched topography of the surface because of the large Young's modulus, reducing the efficiency of charge transport. Both of these trends tend to favor inverse MacEtch (I-MacEtch).[8,9,16]

We first show the I-MacEtch behavior using a conventional liquid phase (LP) MacEtch, presumably because of limited mass transport at the interface between TiN and Si. We then attempted a pseudo-vapor-phase (VP) MacEtch method, slightly modified from the one pioneered by Hildredth et al.[30] aiming to enhance mass transport, which leads to partial forward MacEtch while mostly still dominated by the I-MacEtch behavior. We finally developed a true-VP MacEtch approach, which enabled the fabrication of ordered Si NW arrays with aspect ratio of >5:1 from a TiN mesh-patterned Si wafer. The etch depth as a function of patterned TiN mesh dimension, solution concentration, etching temperature, and TiN film thickness are systematically investigated to characterize and understand the etching behavior of this new catalyst.

RESULTS AND DISCUSSION

TiN I-MacEtch under LP-MacEtch. Compared to Au-MacEtch, the etch rate using TiN as the catalyst is much slower and little etching was observed at room temperature within the process window experimented. All etching results presented below were obtained at elevated temperatures from 50 to 90 °C. Figure 1a shows the conventional LP MacEtch setup schematic and the resulted morphology of a Si wafer covered with a TiN mesh pattern after LP-MacEtching in a solution of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA for 30 min at 70 °C. It can be seen that the exposed Si area in the mesh holes has been etched whereas the Si directly underneath the TiN mesh catalyst remains intact, resulting in the periodic hole array surface textures and revealing the I-MacEtch nature. The I-MacEtch process can also be clearly seen in the cross-sectional scanning electron microscopy (SEM) image of a 5 min LP-MacEtched sample shown in Figure S1 in the Supporting Information. Note that no etching takes place without the presence of TiN, confirming the catalytic nature of TiN for this etching reaction.

It is well known that I-MacEtch results from limited mass transport of the etchant under the metal catalyst.[8−10,31] Under I-MacEtch, the generation of electronic holes from the oxidant at the catalyst surface is faster than the removal of the oxidized Si formed under the catalyst; thus the unconsumed holes localized at the catalyst attract the electrons in areas in between the catalyst, leaving the Si in that region oxidized instead. In the case of the TiN−Si interface, it is known that the adhesion between the two surfaces is extremely strong,[29] so it is highly likely that the etchant has a difficult time to penetrate the interface for etching to continue. Therefore, it is not surprising that TiN catalyzed etching shows I-MacEtch.

Pseudo-VP-MacEtch. In an effort to enhance the mass transport of etchants, we attempted to use a VP etching setup illustrated in Figure 1b, slightly modified from the one pioneered by Hildreth et al. for the demonstration of MacEtch using Au, Ag, Pd/Au catalysts on Si substrates.[30] In this case, the TiN patterned sample was held upside down ∼5 cm above the MacEtch solution. The solution was heated while the substrate was kept at room temperature. The MacEtch takes place when the solution is evaporated and diffused onto the sample surface. The SEM image shows the resulted etching morphology using this setup for an otherwise identical sample

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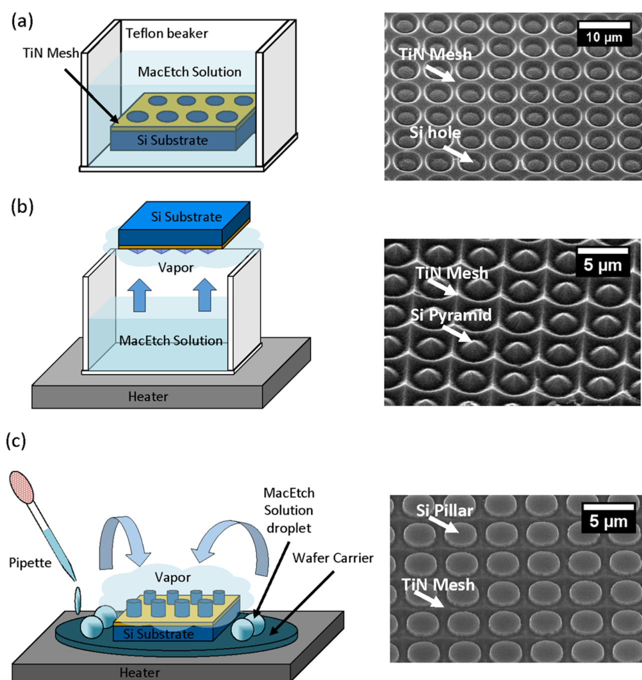

Figure 1. Schematic illustrations of three kinds of MacEtch setups and the corresponding etching morphology of TiN mesh patterned Si substrate shown in 45° tilted SEM images: (a) conventional LP-MacEtch, where the TiN patterned silicon (Si) sample is immersed in solution during etching; Si is preferentially etched inside the TiN mesh holes, leaving behind an indented periodic structure, indicating the I-MacEtch nature. (b) Pseudo-VP MacEtch, where the TiN patterned sample faces down and is separated by a gap from the solution; the material at the edge of the mesh holes are preferentially removed but the center area remains intact, forming periodic pyramids as a result of partial I-MacEtch. (c) True VP-MacEtch, where the TiN patterned Si sample faces up, and the vapor etchant is provided by the solution droplets placed on a heated dummy wafer carrier; materials in the mesh holes are intact whereas areas underneath the mesh are removed, demonstrating successful forward MacEtch.

and etch condition as in Figure 1a, except for only 5 min. The morphology is clearly different from that using the conventional LP-MacEtch in Figure 1a. However, in contrast to 100% forward MacEtch as in the case of Au-catalyzed Si MacEtch,[30] it only resulted in partial forward and partial I-MacEtch: pyramid-shaped pillars with clear facets are formed in the exposed Si (TiN mesh hole) region, whereas the TiN mesh covered region also got etched into ridges. This indicates that this kind of VP-MacEtch is indeed enhancing the mass transport to reduce the inverse etching effect (the center of the mesh hole area remains not etched), but still not sufficient to completely quench the I-MacEtch. We attribute this etching phenomenon to the simultaneous MacEtch reactions in vapor and LPs, because in this setup (Figure 1b), the vapor generated from the heated solution is easily condensed onto the nonheated sample surface, which blocks the mass transport path of the vapor etchant and byproduct species. This method will be denoted as pseudo-VP MacEtch from here on.

True VP-MacEtch. In order to overcome the vapor condensation issue, both the solution and the sample must be heated, ideally at the same temperature. Figure 1c shows the schematic of the modified VP-MacEtch setup and resulted etch morphology of an identical sample and etch condition as in Figure 1b. A dummy 4 in. Si substrate is placed on the hot plate and the TiN mesh-patterned Si sample is placed on top of the heated dummy substrate. Droplets (10 μL) from the premixed MacEtch solution were dispersed on the dummy Si substrate ~1 cm away from the edge of the TiN patterned sample using the micro-pipette. The MacEtch starts when the vaporized MacEtch solution diffuses onto the TiN sample. The solution droplets on the dummy wafer were replenished right after the droplets were completely evaporated. As can be seen from the SEM image, the Si under the TiN mesh is uniformly etched leaving behind flat top pillars in the mesh hole region, demonstrating successful forward MacEtch process using TiN catalyst.

Figure 2a–d shows 52° tilted FIB cross-sectional SEM images showing the resulted etch morphology of VP-MacEtch

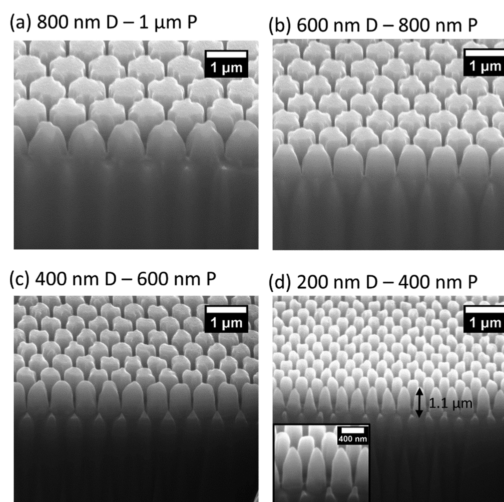

Figure 2. 52° tilted cross-sectional SEM images after FIB, showing the NW array fabricated by true VP-MacEtch with the TiN catalyst mesh pattern hole size of (a) 800 nm diameter, 1 μm pitch (b) 600 nm diameter, 800 nm pitch, (c) 400 nm diameter, 600 nm pitch, and (d) 200 nm diameter, 400 nm pitch.

with the TiN mesh pattern diameter of 800, 600, 400, and 200 nm at fixed spacing of 200 nm in a solution of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA at 90 °C for 5 min. Si under the TiN etches down vertically producing the uniform near-vertical (80°) NW arrays. An aspect ratio of >5:1 is achieved in the 200 nm diameter. Much higher aspect ratio is expected with longer etch time. The rough top surface and slight tapering of the sidewalls of the etched pillars are a result of the etching resulted from diffusion of the unconsumed holes from the TiN pads.

We attribute the well-defined forward MacEtch to the new setup, which enabled the effective VP diffusion of the reactants (HF and H_2O_2) and the etching byproducts (H_2O, H_2SiF_6, and H_2), to ensure continuous cycles of catalyzed oxidation and lateral removal of the oxide at the tight interface of the unique TiN metal catalyst and Si. As in LP-MacEtch, the etch rate is directly affected by the transport of the etchant and byproducts. Importantly, the diffusion in the VP is related to the temperature with order of 3/2 according to the Chapman–Enskog theory,[32] where in LP, the diffusion coefficient of the solution is affected by the dynamic viscosity of the solution linearly according to the Stokes–Einstein equation.[33] Therefore, the mass transport can be significantly enhanced in the

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VP-MacEtch to overcome the limited mass transport resulted from the strong van der Waals force between TiN and the Si substrate.[29] Note that the liquid byproducts (H_2O_2 and H_2SiF_6) need to be evaporated to be diffused to atmosphere whereas the vapor byproducts (H_2, SiF_6) can be diffused as they are produced. When the evaporation rate of the liquid byproducts is slow because of the low substrate temperature, the vapor byproducts can be trapped under the catalyst, which can lead to the delamination or crack of the TiN catalyst film.

Etch Rate Dependence and Activation Energy. We have reported previously[34] etch rate dependence on catalyst mesh diameters and pitch systematically for Au-catalyzed MacEtch previously, confirming the competition between carrier generation and mass transport during the etch process. A similar trend is observed here for TiN-MacEtch, as shown in Figure S2. To explore the temperature-dependent etch rate behavior for TiN-MacEtch, Figure 3a plots the average etch rate of the NW as a function of the TiN catalyst mesh diameter from 200 to 800 nm at a fixed pitch of 1000 nm VP-MacEtched in a solution of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA at varied etching temperatures from 50 to 90 °C for 5 min. At 50 °C, the average NW length stays constant at ∼30 nm when the diameter increases from 400 to 800 nm. As the temperature increases from 50 to 80 °C, the parabola-like NW length trend appears;[34] at 80 °C, the NW length increases from 50 to 460 nm as the diameter increases from 200 to 600 nm and decreases to 210 nm as the diameter further increases to 800 nm. For 60 to 80 °C, the NW length peaks at 600 nm diameter. When the temperature further increases to 90 °C, the NW length continues to increase even when the mesh diameter increases to 800 nm. However, the NW length only increases for diameter from 600 to 800 nm, whereas at the diameter from 200 to 400 nm, the NW lengths are the same as the corresponding ones in 80 °C. The temperature-dependent etch rate trend from 50 to 80 °C can be divided into three regions: the first region is the smallest diameter examined (200 nm) where the etch rate stays constant at a value of 60 ± 9 nm with increasing temperature. We attribute the constant etch rate to be resulting from the limited mass transport because of the large TiN covered space between the small mesh hole (recall that the pitch is fixed). The oxidized Si removal rate enhanced by increasing temperature in this range is insufficient to increase the vertical etching rate. The second region is the middle diameter range (400−600 nm) where the etch rate increases with increasing temperature and increasing diameter. This is because of the balanced carrier generation (oxidation, which increases with diameter) and mass transport (removal, which increases with temperature). The development of the parabola peak (i.e., maximized NW length) at 600 nm diameter indicates that formation of oxidized Si by carrier generation and removal of the oxidized Si by mass transport are both at maximum. The third region is the large diameter range examined (600−800 nm) where the etch rate increases with temperature but decreases with increasing diameter (except at the highest temperature), attributed to the limited carrier generation rate mechanism, leading to the ultimate parabolic rate curve. This is because the amount of holes injected by the carrier generation is reduced by the increased catalyst mesh hole diameter (decrease in TiN area), whereas the oxidized Si removal rate by mass transport is maximized by increasing temperature. The transition from the parabola to linear etching trend at 90 °C not only supports the enhanced carrier generation at 800 nm diameter but also indicates the saturation of the mass transport enhancement with increasing temperature. It can be imagined that if the TiN mesh hole diameter continued to increase, the curve at 90 °C would make a down turn eventually and transition to parabola shape.

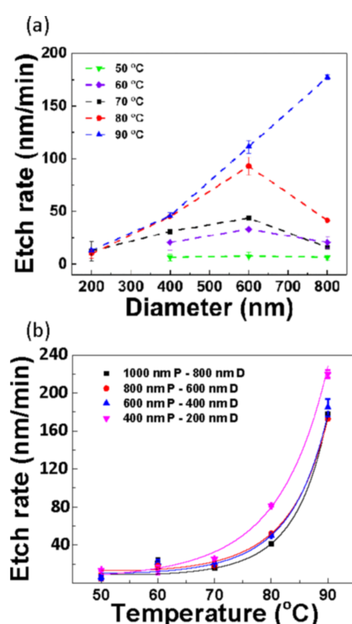

Figure 3. Average etch rate of the NWs using VP-MacEtch with a fixed solution concentration of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA for 5 min, plotted as a function of (a) TiN mesh pattern hole diameter from 200 to 800 nm at a fixed pitch of 1 μm under varied etching temperatures from 50 to 90 °C as labeled and (b) etching temperature at a fixed mesh hole spacing of 100 nm but varied diameter (D) and pitch (P) as labeled.

Figure 3b shows the average etch rate of the NW as the function of etching temperature from 50 to 90 °C for fixed spacing of 100 nm but varied pitch of 400, 600, 800, 1000 nm. It can be seen that the etch rate exponentially increases with increasing temperature. The activation energy of the TiN VP-MacEtch can be calculated by fitting the experimental data to Arrhenius equation as shown in eq 1

$$K = A \times e^{-E_a/(K_B T)} \quad (1)$$

where K is the etch rate, A is the frequency factor, E_a is the activation energy in eV, K_B is the Boltzmann constant, and T is the temperature in K. An activation energy of 0.78 eV is extracted. This indicates that the energy barrier required for TiN to enable forward MacEtch is higher than that for Au catalyzed MacEtch.[5]

Etch Rate Dependence on TiN Thickness. Figure 4a shows the etch rate as a function of TiN mesh diameter from 200 to 800 nm at a fixed pitch of 1 μm for TiN thickness of 5, 10, and 30 nm VP-MacEtched in a solution of 0.28 M HF, 13 mM H_2O_2, and 0.39 M IPA at 80 °C for 5 min. For 5 nm thick TiN, the etch rate decreases gradually from 55 to 12 nm/min as the TiN mesh diameter increases from 400 to 800 nm. As the TiN thickness increases to 10 nm, etch rate increases and the parabola-like dependence on diameter appears with the peak at 600 nm diameter. As the TiN thickness increases to 30 nm, the etch rate for all diameters further increases and the parabola-like trend is clearly shown. Note that the data points for the diameter smaller than 400 nm for 5 and 10 nm thick TiN are missing because the TiN mesh was cracked or

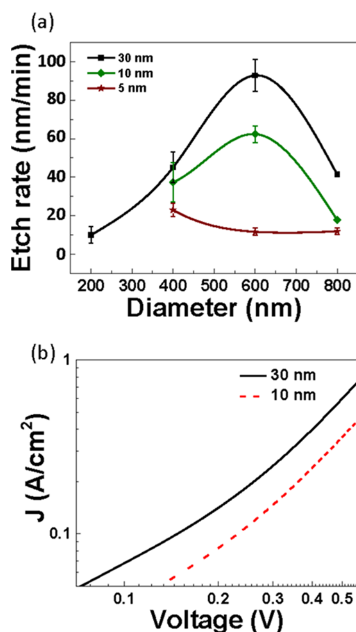

Figure 4. (a) Average etch rate of the NWs as a function of TiN mesh hole size from 200 to 800 nm in diameter at a fixed pitch of 1 μm but varied TiN thickness of 5, 10, and 30 nm, VP-MacEtched with a fixed solution concentration of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA at 80 °C for 5 min, (b) current density as a function of applied voltage for 10 and 30 nm thick TiN on *p*-Si.

delaminated for those samples. One of the hypotheses is that the increase in etch rate with increasing TiN thickness is related to the change in Schottky barrier height (SBH). Figure 4b plots, on a double-log scale, the measured current density using interdigitated finger pads as a function of the bias voltage from 0 to 0.6 V for 10 and 30 nm thick TiN film on the same p-Si plain substrate. The current density increases as the TiN thickness increases from 10 to 30 nm. This can be attributed to the decrease in SBH,[35] because of the decrease of the work function with the increase in TiN thickness.[36] For our case, the extracted SBHs of 30 and 10 nm TiN from the I−V curves are 0.492 and 0.51 eV, respectively (the SBH extraction details can be found in the Supporting Information). This is consistent with the etch rate variation with TiN thickness observed, because the lowering of SBH with the increase of the TiN thickness makes the hole injection rate to Si higher, thus the etch rate faster. However, it is possible that other factors including the adhesion difference as a result of TiN thickness at the TiN−Si interface play a role on the etch rate also.

We note that it is important to understand the role of the heterojunction between the metal catalyst and the semiconductor in MacEtch. Such studies have been carried out previously by several groups including ours.[3,10,21] The barrier height and band alignment between TiN and Si will change as a function of doping concentration, which will lead to change of the carrier confinement at the interface and the balance of charge and mass transport. The balance of charge and mass transport will obviously also vary as a function of the catalyst pattern and dimension, solution concentration, etching temperature, and TiN thickness. They will in turn change the etch rate and localization, and hence morphology. In this case, TiN forms an Schottky contact with p-Si and the band diagram is illustrated in Figure S11. Because of the low SBHs here, the injected holes are not completely trapped at the interface. In general, porosity occurs if the SBH is not high enough to confine the carriers where they are generated.[10,37,38] Although not the focus of this paper, the formation of porous morphology was observed, especially increased as the pillar diameter decreases at a fixed pitch, as shown in Figures S2−S9, because of the oversupply of carriers under limited mass transport condition. By enhancing the mass transport and/or reducing the carrier generation rate, through optimizing the HF to H_2O_2 concentration ratio (Figure S12) as a function the TiN pattern, thickness, and Si doping levels, the porosity can be minimized. It is also possible to remove the porosity by post-MacEtch digital etching as previously demonstrated for InGaAs.[10] Note that even if it has some porosity, CMOS-compatible catalyst enabled MacEtch can still be used for gate poly etch or any other silicon-related etching process as long as it does not impact the CMOS interface. Nonetheless, for future studies, a dedicated VP-MacEtch setup that allows programmable control of the flow of individual etchant, sample temperature, and chamber pressure will be used for systematic mapping of a much bigger parameter space than reported here to scale the etch rate and aspect ratio, as well as porosity.

CONCLUSIONS

We have demonstrated CMOS-compatible TiN-assisted chemical Etching of Si. We have found that the mass transport in TiN−Si MacEtch is strongly limited as compared to the conventional Au−Si MacEtch under the same etch condition, presumably because of the stronger adhesion property of TiN to Si. Under conventional LP MacEtch condition, areas in the TiN mesh holes are chemically etched producing the I-MacEtched structures. The pseudo-VP-MacEtch resulted in partial forward MacEtch because of vapor condensation on the sample surface by the temperature difference between the substrate and solution vapor. Using the true VP-MacEtch scheme reported here by fixing the substrate and vapor temperature the same, the transition from inverse to forward MacEtch is completed via total VP reaction. The vertical etch rate as a function of TiN mesh dimension, H_2O_2 concentration, etching temperature, and TiN thickness are systematically characterized with the true VP-MacEtch, confirming the MacEtch mechanism dictated by the carrier generation and mass transport processes. Si NW arrays with aspect ratio >5:1 is realized. The demonstration of producing high aspect ratio Si structures with TiN catalyst shows that MacEtch is not limited to non-CMOS-compatible noble metals and this allows MacEtch to be applied in device applications that are sensitive to deep-level defects. In addition, TiN-MacEtch demonstrated here, which leaves the TiN film embedded in the surface of 3D Si structures, may also have direct implications in TiN-based plasmonic semiconductor structures for photonic applications.[39,40]

In summary, this work represents a significant first step toward taking the disruptive MacEtch technique to CMOS-compatible commercial applications. Furthermore, transforming solution based MacEtch to VP MacEtch while maintaining the damage free nature holds great potential to controllability and scalability for manufacturing.

EXPERIMENTAL SECTION

Boron-doped p-Si single crystal (100) substrates with resistivity of 1−100 Ω cm were used for all experiments. After native oxide etching in 1:100 HF/DI for 60 s, the substrates were deposited with 5, 10, 30 nm TiN using physical vapor deposition by Lam Research

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Corporation (LRCX). Then, 15 nm SiO_2 hard mask was deposited using PECVD (Trion Minilock—Orion PECVD system). Electron beam resist of 950 k poly(methyl methacrylate) (PMMA) in 2% anisole was spin-coated at 2000 rpm for 60 s (~80 nm thickness) and baked at 200 °C for 2 min. Patterns consist of hexagonal ordered dot arrays with diameters varying from 200, 400, 800 nm at pitches of 400, 600, 800, 1000 nm were exposed using electron beam lithography and developed in 1:3 MIBK/IPA for 2 min.

The patterns were transferred on the SiO_2 hard mask by etching in 1:10 buffered oxide etchant (BOE) for 15 s. The PMMA was removed in 5 min cycles in aceton, methanol, and IPA. Then, the residual PMMA was etched by O_2 RIE at 200 mw for 2 min. The exposed TiN patterns were etched in 1:10 NH_4OH/H_2O_2 (~15 nm/min). The SiO_2 hard mask was etched in 1:10 BOE for 15 s.

The VP-MacEtch was carried out after the sample patterning. First, a 4 in. dummy Si substrate was placed on the hot plate to serve as a wafer carrier. Then, the TiN patterned Si sample was placed on the center of the wafer carrier. The surface temperature of the wafer carrier and the TiN patterned Si sample were calibrated to match the etching temperature (50, 60, 70, 80, 90 °C). The maximum temperature of 90 °C was chosen only based on the limitation from the experimental setup used, where the MacEtch solution was dispensed onto the wafer carrier manually. At >90 °C, the MacEtch solution evaporated immediately such that it made it difficult to control the continuous generation of vapor around the sample. The MacEtch solution of 0.28 M HF, 13 mM H_2O_2, 0.39 M IPA was mixed. The 10 μL solution was dropped on the wafer carrier around the TiN patterned Si sample using an HF-resistive micro-pipette. A total of 6−8 pipettes of solutions were dropped on the carrier ~2 cm away from the TiN patterned Si sample. The solution was replenished soon after the drops were completely evaporated. Five samples were etched for each given condition. The VP-MacEtched samples were inspected using a secondary electron microscope (SEM, Hitachi S-4800). No degradation of the TiN mask was observed under all etching conditions for the duration specified. The average NW heights were measured from the 45° tilted SEM images. The height and aspect ratio NWs at the given etching time were inspected by the 52° tilted images after the cross-sectional ion milling using the focused ion beam (FEI-DB4800).

For the current density measurement sample, 15 nm SiO_2 by PECVD was deposited onto the same p-Si substrates with 5, 10, and 30 nm thick TiN used for etching. Then, hexamethyldisilane and PR were spin-coated at 4500 rpm for 30 s, respectively, followed by baking at 110 °C for 1 min. An interdigitated pad pattern, with the electrode fingers of 8 μm in width, 26 μm in spacing, and 290 μm in length, was exposed using Karl Suss MJB-3 aligner at 270 mW for 1 min and developed in AZ 917 MIF developer for 2 min. The pattern was then transferred onto SiO_2 by etching in BOE for 15 s. After removing PR in acetone, methanol, IPA cycles, the pattern on the SiO_2 was transferred onto TiN by etching in 1:10 NH_4OH/H_2O_2. Then, I-V curves were measured using Keithley 4200 parameter analyzer and the current density was calculated by dividing the measured current by the area of the TiN interdigitated pads.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b00871.

> I-MacEtch of the TiN sample in the conventional LP MacEtch; SEM images of VP MacEtched NWs as a function of mesh dimension, solution concentration, etching temperature, and TiN thickness; Schottky barrier height extraction of 30 and 10 nm TiN on Si; band diagram of TiN and p-type Si junction; and tunability of porosity: effect of H_2O_2 concentration on the porosity of Si nanostructures (PDF)

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Notes

The authors declare no competing financial interest.

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